WHAT IS CLAIMED IS:

1. A method of imaging features onto a wafer comprising:

establishing a grid having grid pitches;

arranging a plurality of real features on the grid;

creating one mask, the mask including all of the plurality of real features and a plurality of assist features, the assist features being sized such that they do not print while allowing an illumination to be optimized; and

imaging the real features onto a wafer.

2. The method of imaging features according to claim 1, wherein the assist features are introduced at grid points that do not have any of the plurality of real features.

3. The method of imaging features according to claim 1 wherein the grid has a grid pitch p_x in a direction and a grid pitch p_y in a perpendicular direction.

4. The method of imaging features according to claim 1 wherein grid pitches, p_x and p_y, are selected to minimize circuit area.

5. The method of imaging features onto a wafer according to claim 3, wherein the grid pitches in two perpendicular directions, p_x and p_y, are smaller than a minimum pitch of single-exposure lithography.

6. The method of imaging features according to claim 5, wherein a distance between two adjacent real features is no less than the minimum pitch of single-exposure lithography.

7. A method of imaging features onto a wafer comprising:

establishing a grid having grid pitches;

arranging a plurality of real features on the grid;

arranging a plurality of assist features on the grid points;

creating two masks, the first mask including a first subset of the plurality of real features and a first subset of the plurality of assist features, the second mask containing a second subset of the plurality of real features and a second subset of the plurality of assist features, the assist features being sized such that they do not print but nevertheless create a mask spectrum that allows an illumination to be optimized; and

imaging the real features onto the wafer.

8. The method of imaging features according to claim 7 wherein the grid has a grid pitch p_x in a direction and a grid pitch p_y in a perpendicular direction.

9. The method of imaging features according to claim 7, wherein grid pitches, p_x and p_y, are selected to minimize circuit area.

10. The method of imaging features according to claim 7, wherein the assist features are arranged on the grid points that do not have a real feature.

11. The method of imaging features onto a wafer according to claim 7, wherein the grid pitches in two perpendicular directions, p_x and p_y, are smaller than a minimum pitch of single-exposure lithography.

12. The method of imaging features onto a wafer according to claim 11, wherein a distance between two adjacent real features is no less than the minimum pitch of single-exposure lithography.

13. A method of imaging features onto a wafer according to claim 7, wherein the first and second masks are sequentially exposed to print the features.

14. The lithography method according to claim 7, wherein the distance between two adjacent real features is no less than the minimum pitch of single-exposure lithography while the grid pitches in two perpendicular directions, p_x and p_y, are smaller than the minimum pitch of single-exposure lithography.

15. The lithography method according to claim 14, wherein a diagonal distance between two adjacent features (real or assist features) is $\sqrt{p_x^2 + p_y^2}$ where p_x is the pitch between two adjacent features (real or assist features) in an x direction and p_y is the pitch between t two adjacent features (real or assist features) in a perpendicular direction of an x direction.

16. A mask set for imaging a die comprising:

a first mask, the first masking having a first set of real features and a first set of assist features; and

a second mask having a second set of real features and a second set of assist features,

wherein two adjacent features (real or assist features) in the first or second mask are spaced at no less than a minimum pitch for single-exposure lithography.

17 The mask set according to claim 16, wherein the first set of real features and the second set of real features create a set of real features for a single die.

18. A mask set for imaging a die according to claim 16, wherein the first set of real features is distinct from the second set of real features.

19. A mask set for imaging a die according to claim 16, wherein the first set of assist contacts is distinct from the second set of assist contacts.

20. The mask set for imaging a die according to claim 16, wherein a diagonal distance between two neighboring features (real or assist features) is $\sqrt{p_x^2 + p_y^2}$ where p_x is the pitch between two adjacent features (real or assist features) in an x direction and p_y is the pitch between two adjacent features (real or assist features) in the perpendicular direction of an x direction.

21. A method of imaging features onto a wafer comprising:

establishing a grid having a grid pitch;

arranging a plurality of real features on the grid;

creating at least one mask, the mask including at least one real feature and a plurality of assist features, the assist features being sized such that they do not print while allowing an illumination to be optimized; and

imaging the real feature onto a wafer.

22. The method of imaging features according to claim 21, wherein the assist features are introduced at grid points that do not have any of the plurality of real features.

23. The method of imaging features according to claim 21 wherein the grid has a grid pitch p_x in a direction and a grid pitch p_y in a perpendicular direction.

24. The method of imaging features according to claim 21 wherein grid pitches, p_x and p_y, are selected to minimize circuit area.

25. The method of imaging features onto a wafer according to claim 23, wherein the grid pitches in two perpendicular directions, p_x and p_y, are smaller than the minimum pitch of single-exposure lithography.

26. The method of imaging features according to claim 25, wherein a distance between two adjacent real features is no less than a minimum pitch of single-exposure lithography.

27. A method of imaging features onto a wafer comprising:

establishing a grid having a grid pitch;

arranging a plurality of features on the grid;

arranging a plurality of assist features on the grid points;

creating at least two masks, the first mask including a first subset of the plurality of features and a first subset of the plurality of assist features, the second mask containing a second subset of the plurality of features and a second subset of the plurality of assist features, the assist features being sized such that they do not print but nevertheless create a mask spectrum that allows an illumination to be optimized; and

imaging the features onto the wafer.

28. The method of imaging features according to claim 27, wherein the assist features are introduced at grid points that do not have any of the plurality of real features.

29. The method of imaging features according to claim 27 wherein the grid has a grid pitch p_x in a direction and a grid pitch p_y in a perpendicular direction.

30. The method of imaging features according to claim 27 wherein grid pitches, p_x and p_y, are selected to minimize circuit area.

31. The method of imaging features onto a wafer according to claim 29, wherein the grid pitches in two perpendicular directions, p_x and p_y, are smaller than the minimum pitch of single-exposure lithography.

32. The method of imaging features according to claim 31, wherein a distance between two adjacent real features is no less than a minimum pitch of single-exposure lithography.